min. to about 75 min. The thickness of the electroplated metal or alloy is typically about 25μ to about 200μ, and more typically about 40μ to about 75μ.

In the case of exposed α-Ta, the metal being plated will not plate on the barrier layer due to the formation of a very thin oxide layer when contacting the electroplating bath. The oxide layer may be described as a "superficial" layer. This oxide layer will form naturally if the barrier layer is a tantalum layer such as that described above. In another embodiment, the oxide layer may be formed by momentarily reversing the polarity of the field, rendering the workpiece anodic, prior to the electroplating. The polarity change may be brief, such as about 10 seconds. Formation of the oxide layer may also be described as "anodization". The current density should be such that at the end of the current reversal, sufficient copper is left in the recesses for plating to initiate.

Next, the barrier layer **11** may be removed down to the polyimide or polyimide passivation layer, after the solder reflow. The barrier layer may be removed by utilizing the electroplated metal as a mask.

According to the process of the present invention, no lithograph step is required to define the seed layer since the chemical-mechanical polishing step makes the seed layer self-aligning to the recess(es). Not requiring a lithographic step simplifies the process. Additionally, the process may be less costly as compared to typical lithographically defined C4 processes. This simplification and cost advantage may be realized in any process requiring similar selective plating of metal(s).

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention but, as mentioned above, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.

What is claimed is:

1. A method for plating a second metal directly to a first metal, said method comprising the steps of:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

depositing a photoresist layer over said plating seed layer;

removing portions of said photoresist layer and portions of said plating seed layer outside of said at least one recess;

removing photoresist remaining in said at least one recess; and

electroplating a second metal to said plating seed layer in said recess without utilizing a mask.

2. The method according to claim **1**, wherein said metal feature is a metal last provided in said semiconductor substrate.

3. The method according to claim **1**, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the layer including the nitride of tantalum is in the α-phase.

4. The method according to claim **3**, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

5. The method according to claim **1**, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

6. The method according to claim **5**, wherein said seed layer is copper.

7. The method according to claim **6**, wherein said copper is sputter coated on said layer of tantalum.

8. The method according to claim **7**, wherein said layer of tantalum is α-Ta/TaN layer.

9. The method according to claim **6**, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

10. The method according to claim **3**, wherein said tantalum is alpha tantalum.

11. The method of claim **3**, wherein said tantalum layer is TaN/α-Ta/TaN-laminate.

12. The method according to claim **1**, wherein said portions of said photoresist layer and said seed layer outside of said recess are removed by chemical-mechanical polishing.

13. The method according to claim **1**, wherein said photoresist is spun on said plating seed layer.

14. The method according to claim **1**, wherein said barrier layer forms a conductor for said electroplating of said second metal.

15. The method according to claim **1**, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.

16. The method according to claim **1**, further comprising the step of:

removing said at least one conductive barrier layer from horizontal portions between said recesses.

17. The method according to claim **16**, wherein said electroplated second metal acts as a mask for the removal of said at least one conductive barrier layer.

18. The method according to claim **1**, wherein said at least one metal feature is formed in said substrate.

19. The method according to claim **1**, wherein said insulating layer includes a layer of an oxide and a nitride and at least one layer of a polyimide.

20. The method of claim **19**, further comprising the step of:

forming a layer of at least one nitride or other passivation layer over the polyimide.

21. The method according to claim **1**, wherein said second metal is a solder ball.

22. A method for plating a second metal directly to a first metal, said method comprising the steps of:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

providing a pad in said at least one recess for preventing removal of portions of said seed layer in said at least one recess;

removing portions of said plating seed layer outside of said at least one recess;

removing said pad; and

electroplating a second metal to said plating seed layer in said recess without utilizing a mask.

23. The method of claim **22**, further comprising the step of:

utilizing a hard polishing pad to remove said seed layer outside of said recess.

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